Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **S3**
2. **D3**
3. **D1**
4. **S1**
5. **IN1**
6. **V+**
7. **GND**
8. **V-**
9. **IN2**
10. **S2**
11. **D2**
12. **D4**
13. **S4**
14. **V+**

**.100”**

**.096”**

**1 14 13**

**2**

**3**

**4**

**5**

**6 7 8**

**12**

**11**

**10**

**9**

**AG37Y**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: AG37Y**

**APPROVED BY: DK DIE SIZE .096” X .100” DATE: 11/23/16**

**MFG: MAXIM THICKNESS .012” P/N: DG303AC/D**

**DG 10.1.2**

#### Rev B, 7/19/02